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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,119	06/27/2003	Holly G. Gates	INK-109	6703

26245 7590 05/19/2006

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,119	GATES, HOLLY G.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *38-40,50,53,54 and 57-60* is/are rejected.

7)☒ Claim(s) *41-49,51,52,55 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11-6-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 38-41, 50, 53-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Proebsting (US Patent No. 5,952,948).

As to claim 38, Proebsting teaches an addressing structure for addressing a display medium (See Col. 1, Lines 5-9), the structure comprising:

a plurality of column electrodes, each of the column electrodes being connected via switch means to a plurality of pixel electrodes (See Fig. 1, items 110, 112, Col. 1, Lines 57-59);

a plurality of voltage sources each having a different voltage level (See Figs. 2-3, items 6.4 v, 6.3 v, ..., Col. 2, Lines 3-24); and

a switch unit having a plurality of voltage source inputs each connected to one of the plurality of voltage sources, and a plurality of outputs each connected to one of the plurality of column electrodes, the switch unit being capable of connecting each of the column electrodes independently to selected ones of the plurality of voltage sources (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-4, item 204-8, Col. 2, Lines 29-33).

As to claims 39, 41 Proebsting teaches switch unit further comprises at least one display signal input arranged to receive a display signal specifying the voltage to be placed upon the column electrodes, and the switch unit is arranged to connect each of

the column electrodes independently to selected ones of the plurality of voltage sources dependent upon the display signal (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-4, item 204-8, Col. 2, Lines 29-33).

As to claim 40, Proebsting teaches switch unit comprises one display signal input (See Fig. 1, item 100) for each column electrode and the switch unit is arranged to connect each column electrode to a selected one of the plurality of voltage sources dependent upon the display signal received by the display signal input associated with the column electrode (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-3, item 204-8, Col. 2, Lines 29-33).

As to claim 50, Proebsting teaches an electro-optic display comprising:

an addressing structure according to claim 38 (See rejection of claim 38); and

an electro-optic medium disposed between the pixel electrodes of the addressing structure and the second layer (See Fig. 1, item 108, Col. 1, Lines 9-15).

It is inherent in LCD panel to have a transparent substrate bearing a single transparent common electrode, the common electrode extending across all the pixels of the display

As to claim 53, Proebsting teaches a method for addressing a display medium (See Col. 1, Lines 5-9), the method comprising:

providing a plurality of column electrodes, each of the column electrodes being connected via switch means to a plurality of pixel electrodes, the pixel electrodes

being arranged to apply electric field to pixels of the display medium (See Fig. 1, items 110, 112, Col. 1, Lines 57-59);

providing a plurality of voltage sources each having a different voltage level (See Figs. 2-3, items 6.4 v, 6.3 v, ..., Col. 2, Lines 3-24); and

providing a switch unit having a plurality of voltage source inputs each connected to one of the plurality of voltage sources, and a plurality of outputs each connected to one of the plurality of column electrodes, the switch unit further comprising a display signal input arranged to receive a display signal (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-4, item 204-8, Col. 2, Lines 29-33),

by means of the switch unit connecting each of the column electrodes independently to selected ones of the plurality of voltage sources, the voltage source connected to each column electrode being controlled by the display signal (See Fig. 1, items 100, 102, 104, 106 and Figs. 2-4, item 204-8, Col. 2, Lines 29-33).

As to claim 54, Proebsting teaches receiving in a data register (See Fig. 1, item 102) data representing the voltages to be applied to each of the column electrodes, storing said data in said data register (See Fig. 1, item 102) , transferring said data to a data latching means (See Fig. 1, item 104) , and generating the display signal dependent upon the data in the data latching means (See Figs. 1-3, items 100, 102, 104, 106).

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 57-60 are rejected under 35 U.S.C. 102(e) as being anticipated by Katase (US Patent No. 7,019889).

As to claim 57, Katase teaches a method for addressing a display medium (See Col. 1, Lines 11-14), the method comprising:

providing a first column electrode (See Fig.1,item X1), a first pixel electrode (See Fig.1,item 104), a first capacitor connected to the first pixel electrode (in the reference capacitor formed by items 1,104,201) (Fig. 2, items 1,104,201, Col. 9, Lines 20-24), and a first resistive switch means having an open position in which the first column electrode is not connected to the first pixel electrode (See Fig.1,item 103), and a closed position in which the first column electrode is connected via a resistance (on resistance of TFT) to the first pixel electrode (See Fig.1,item 103);

providing a second column electrode (See Fig.1,item X2), a second pixel electrode (See Fig.1,item 104), a second capacitor connected to the second pixel electrode (in the reference capacitor formed by items 1,104,201) (Fig. 2, items 1,104,201, Col. 9, Lines 20-24), and a second resistive switch means having an open position in which the second column electrode is not connected to the second pixel electrode (in the reference capacitor formed by items 1,104,201) (Fig. 2, items 1,104, 201, Col. 9, Lines 20-24), and a closed position in which the second column electrode is connected via a resistance (on resistance of TFT) to the second pixel electrode (See Fig.1,item 103);

placing both the first and second switch means in their closed positions,

thereby connecting the first and second column electrodes to the first and second pixel electrodes respectively (See Fig. 1, items 101,103, X1, X2, Col. 9, Lines 29-39);

applying a drive voltage to the first column electrode for a first period of time, thereby charging the first capacitor to a first addressing voltage different from the drive voltage (the drive voltage is 111111) (See Fig. 1, item X1) and Fig. 9, item 000001, Col. 11, Lines 34-41); and

applying the drive voltage to the second column electrode for a second period of time, thereby charging the second capacitor to a second addressing voltage different from both the drive voltage (the drive voltage is 111111) and the first addressing voltage (the first addressing voltage is 000001) (See Fig. 1, item X2) and Fig. 9, item 000010, Col. 11, Lines 34-41).

As to claim 59, Katase teaches an addressing structure for addressing a display medium (See Col. 1, Lines 11-14), the method comprising:

a first column electrode (See Fig.1,item X1), a first pixel electrode (See Fig.1,item 104), a first capacitor connected to the first pixel electrode (in the reference capacitor formed by items 1,104,201) (Fig. 2, items 1,104,201, Col. 9, Lines 20-24), and a first resistive switch means having an open position in which the first column electrode is not connected to the first pixel electrode (See Fig.1,item 103), and a closed position in which the first column electrode is connected via a resistance (on resistance of TFT) to the first pixel electrode (See Fig.1,item 103);

a second column electrode (See Fig.1,item X2), a second pixel electrode (See Fig.1,item 104), a second capacitor connected to the second pixel electrode (in the

reference capacitor formed by items 1,104,201) (Fig. 2, items 1,104,201, Col. 9, Lines 20-24), and a second resistive switch means having an open position in which the second column electrode is not connected to the second pixel electrode (in the reference capacitor formed by items 1,104,201) (Fig. 2, items 1,104, 201, Col. 9, Lines 20-24), and a closed position in which the second column electrode is connected via a resistance (on resistance of TFT) to the second pixel electrode (See Fig.1,item 103);

switch control means arranged to move the first and second switch means in their closed positions, (See Fig. 1, items 101,103, X1, X2, Col. 9, Lines 29-39);

applying a drive voltage to the first column electrode for a first period of time, thereby charging the first capacitor to a first addressing voltage different from the drive voltage (the drive voltage is 111111) (See Fig. 1, item X1) and Fig. 9, item 000001, Col. 11, Lines 34-41); and

voltage supply means arranged to place a driving voltage on the first and second column electrodes while the first and second switch means are in their closed positions, the voltage supply means (the drive voltage is 111111) being capable of applying the drive voltage to the first column electrode for a first period (See Fig. 1, item X1) and Fig. 9, item 000001, Col. 11, Lines 34-41) and of applying the drive voltage to the second column electrode for a second period different from the first period (See Fig. 1, item X2) and Fig. 9, item 000010, Col. 11, Lines 34-41).

As to claims 58 and 60, Katase teaches the first (See Fig. 9, item 000001) and second period (See Fig. 9, item 000010) are multiples of a predetermined interval (See Fig. 9, item 111111, Co. 9, Lines 29-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting as applied to claims 1, 17, 24 in view of White et al. (US Patent No. 4,499,488).

As to claim 42, Proebsting does not disclose multiplexing unit with number of switches equal to the number of voltage sources, in each multiplexing unit only one of the switches is closed at any given time, all the other switches being open.

White et al. teaches multiplexing unit with number of switches equal to the number of cells, in each multiplexing unit only one of the switches is closed at any given time, all the other switches being open (See Fig. 8, items 226,228, Col. 12, Lines 30-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of White et al. into Proebsting system in order to simplify the circuit arrangement.

Allowable Subject Matter

4. Claims 43-44, 51-52, 55-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 43, 51, 55 the major difference between the teaching of the prior art of record (Proebsting and White et al.) and the instant invention is that the switch unit further comprises a blanking signal input arranged to receive a blanking signal, the switch unit being arranged to that, upon receipt of the blanking signal, all column electrodes are connected to the same voltage source.

Relative to claims 44, 52, 56 the major difference between the teaching of the prior art of record (Proebsting and White et al.) and the instant invention is that switch unit comprises a primary switch unit, a plurality of voltage rails, a plurality of secondary switch units each having an output connected to one column electrode, and sequencing means, the primary switch unit having voltage source inputs connected to the voltage source inputs of the switch unit, voltage rail outputs each connected to one voltage rail, and at least one control signal input arranged to receive a primary switch unit control signal from the sequencing means, each secondary switch unit having voltage rail inputs connected to each of the voltage rails and a control signal input arranged to receive a secondary switch unit control signal from the sequencing means, the sequencing means controlling the primary switch unit so that the voltage rails are connected to a first subset of the voltage source inputs of the primary switch unit during a first period, and to a second subset, different from said first subset, of the voltage source inputs of the primary switch unit during a second period, and each of the

secondary switch units being arranged to connect their associated column electrode to a selected one of the voltage rails dependent upon the secondary switch unit control signal.

Claims 45-49 depend on claim 44.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LS
06.12.06

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